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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,812	11/24/2003	Jung S. Kang	42P17606	5364

7590 08/16/2006

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EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,812	KANG ET AL.	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *1-8,13,14,21,22 and 25-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12,15-20,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-48* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the RCE and amendment filed 8/3/06.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9-12, 15-20, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pasch (US005821624A).

Pasch teaches the device of claims 9-12, 15-20 and 23-24 except for explicitly teaching the passive device is a thin film device.

Regarding claim 9, Pasch teaches a passive element (column 24 lines 39-41) between upper and lower dies (column 25 lines 22-24, substrate/interposer (spacer)/die stack, column 23 lines 7-8, substrate may be another die), and conductors attached to the passive element to at least one of the upper and lower dies (column 24 lines 53-58). Regarding the limitation that the passive element is a thin film passive element, Pasch does not teach this directly, but does suggest this. Column 37 teaches that the interposer is rather thin, thus suggesting only a thin film device may be integrated on the

interposer. Column 19 lines 65 to column 20 line 6, teaches that passive or active devices including thin film transistors, resistors, capacitors, inductors, diodes, and varistors may be integrated on the interposer. Thus, as the element is embedded into a thin interposer, and that Pasch teaches a thin film transistor as an embedded device, one skilled in the art would know that the passive devices listed would include those of thin film passive devices.

Regarding the limitation of a package substrate, Pasch teaches a flip-chip assembly is a type of package assembly and Pasch refers to the assembly as such (column 1 lines 55-58, 64, and column 23 lines 24-25).

Regarding claim 10, adhesive layers are filled between the spacer (interposer) and the upper and lower dies (column 25 lines 22-24). Pasch also teaches the die may be attached by solder balls or epoxy or polymer (thus adhesives) to attach the upper and lower dies (column 7 lines 10-11).

Regarding claim 11, the element may be a thin film (column 26 line 16, thin metal film, and as above, the thin film may also be a another passive device). Figure 12b shows the passive element between the spacer and the lower adhesive layer.

Regarding claim 12, the passive device is substantially thinner than the thickness of the spacer (figure 12A).

Regarding claim 15, the passive element may be electrically connected to the upper or lower dies using bumps (column 26 lines 10-16).

Regarding claim 16, the lower die may be attached to a substrate using an adhesive (column 25 lines 19-20).

Regarding claim 17, Pasch teaches a package substrate (column 23 lines 24-26), a plurality of stacked dies (figure 11B), a spacer assembly between the upper and lower dies having a passive element (column 24 lines 39-41) between upper and lower dies (column 25 lines 22-24, substrate/interposer (spacer)/die stack, column 23 lines 7-8, substrate may be another die), and conductors attached to the passive element to at least one of the upper and lower dies (column 24 lines 53-58).
Regarding the limitation that the passive element is a thin film passive element, Pasch does not teach this directly, but does suggest this. Column 37 teaches that the interposer is rather thin, thus suggesting only a thin film device may be integrated on the interposer. Column 19 lines 65 to column 20 line 6, teaches that passive or active devices including thin film transistors, resistors, capacitors, inductors, diodes, and varistors may be integrated on the interposer. Thus, as the element is embedded into a thin interposer, and that Pasch teaches a thin film transistor as an embedded device, one skilled in the art would know that the passive devices listed would include those of thin film passive devices.

Regarding claim 18, adhesive layers are filled between the spacer (interposer) and the upper and lower dies (column 25 lines 22-24). Pasch also teaches the die may be attached by solder balls or epoxy or polymer (thus adhesives) to attach the upper and lower dies (column 7 lines 10-11).

Regarding claim 19, the element may be a thin film (column 26 line 16, thin metal film, and as above, the thin film may also be a another passive device). Figure 12b shows the passive element between the spacer and the lower adhesive layer.

Regarding claim 20, the passive device is substantially thinner than the thickness of the spacer (figure 12A).

Regarding claim 23, the passive element may be electrically connected to the upper or lower dies using bumps (column 26 lines 10-16).

Regarding claim 24, the lower die may be attached to a substrate using an adhesive (column 25 lines 19-20).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Pasch to include thin film passive devices as column 19 line 65 to column 20 line 6, teaches that passive or active devices including thin film transistors, resistors, capacitors, inductors, diodes, and varistors may be integrated on the interposer. Thus,

as the element is embedded into a thin interposer, and that Pasch teaches a thin film transistor as an embedded device, one skilled in the art would know that the passive devices listed would include those of thin film passive devices.

Response to Arguments

3. Applicant's arguments with respect to claims 9-12, 15-20 and 23-24 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the argument over the restriction requirement, in the paper filed 9/22/06, the applicant elected the generic species of a passive element and not either of the more specific species of an inductor or a resistor. Whereas a passive element may be a resistor or capacitor or inductor, the applicant chose the generic term, rather than a species of the passive element, nor made a statement that the different and alternate species were obvious variants. The restriction was proper, and based upon the election, withdrawing claims directed toward a non-elected species (named or described) was also proper.

Regarding the argument that Pasch teaches a flip-chip assembly and this is not a package substrate, the examiner disagrees, a flip-chip assembly is a type of package assembly and Pasch refers to the assembly as such (column 1 lines 55-58, 64, and column 23 lines 24-25).

Regarding the argument that Pasch does not teach a thin film passive element, the examiner contends that this is suggested by Pasch as in the rejections above.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

August 9, 2006